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10/780,967	02/18/2004	Darren John Cepulis	200314546-1	1689

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EXAMINER	
STEELMAN, MARY J	
ART UNIT	**PAPER NUMBER**
2191	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,967	CEPULIS, DARREN JOHN	
	Examiner	Art Unit	
	MARY STEELMAN	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MARY STEELMAN
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Claim Amendments and Remarks received 08/06/2007. Per Applicant's request, claims 1, 11, 19, 22, 24, 29, 30, and 33 are amended. Claims 1-33 are pending.

Claim Rejections - 35 USC § 101

2. In view of the amendment to claim 11, the prior 35 U.S.C. 101 rejections are hereby withdrawn.

Response to Arguments

3. Applicant has argued, in substance, the following:

(A) As noted on page 12 (middle), "Corti et al. apparently does not teach or fairly suggest a process and a debugger program (embedded in a ROM and operating on instructions of the process), both of which run on the same processor (or executing means), as called for in the amended independent claims 1, 11, 19, 22, 24, 29, 30, and 33."

Examiner's Response:

See FIG. 1 & 2. Corti disclosed a System on a Chip (SOC), 12. Col. 3: 9-16, The on-chip logic analyzer (OCLA)...is a system for testing and debugging real-time system-on-chip (SOC) systems, e.g., digital signal processing chips..." Col. 3: 27-36, "on-chip VHDL macro 14 (embedded debugger program) embedded in an SOC device 12 (i.e., a target system)...The SOC device 12 includes a signal processing logic (i.e., DSP core / DSP processor) (processor /

executing means running a process), memory blocks..." Conti disclosed a process and a debugger program, both of which run on the same processor, the SOC, signal processor / signal processing logic.

(B) Corti et al. also apparently does not teach or fairly suggest a disassembler and a trace capturer (or disassembling means or trace means) that are executable by the processor (or executing means), called for in amended independent claims 22, 24, and 30.

Examiner's Response:

Corti disclosed (col. 3: 43-52), "a data capturing unit 21 (trace capturer / trace means)...a trace buffer 24...Upon power-on, the control logic 20 receives control signals designating a mode, a mask value and a match data and a command word..." Col. 3: 53-57, "Once the 'run' bit is the command word is set, the OCLA system 10 starts monitoring the operations of the VHDL macro 14 for trigger conditions...the control logic 20 controls the trace buffer 24... (executable by the processor, DSP core 28) Col. 5: 66 – col. 6: 17 & FIG. 3, "...loads the current mode and associated trigger match and mask values...achieved by loading a trigger word including three 256 bit data words and one command byte...loading of the first trigger word 3a sets an "A" match value, and the second trigger word 3b holds an "a" mask value. These trigger words 3a, 3b are used to bring important signals out of the DSP core (disassembler) 28 into the data capturing unit 21. Corti fairly teaches a processor (DSP core 28) that executes a disassembler and trace capturer.

Applicant argues (page 11) that Corti appears to teach a system on a chip (SOC) with an on-chip logic analysis (OCLA) unit that is a hardware component on the chip that is completely separate from the components of the chip that the OCLA unit is monitoring. By being separate from the monitored component (i.e. the DSP core logic), but integrated on the same chip as the monitored component, the OCLA unit can provide real-time data acquisition without interrupting operations of the monitored component. Applicant further points out that the disadvantage is the required space on the chip. Claim language does not preclude Corti from being an analogous art.

4. Applicant's arguments filed 08/06/2007 have been fully considered but they are not persuasive. Examiner maintains the rejection of claims 1-33.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5, 7-13, 15-26, and 28-33 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,834,360B2 to Corti et al.

Per claim 1:

A method for debugging a computer system, comprising:

-initiating a process in the computer system, the process including instructions and running on a processor in the computer system;

-launching a debugger program that is embedded in a ROM of the computer system, the debugger program running on the processor;

-executing at least part of the instructions by the processor;

-the debugger program operating on at least part of the executed instructions.

Corti: Col. 1: 57-60, 63, on-chip logic analysis system for testing and debugging for the SOC signal processing systems without interrupting operations thereof, real time data acquisition capability Col. 3: 49-52, Upon power-on, the control logic 20 receives control signals designating a mode, a mask value and a match data and a command word (initiating a process / launching a debugger program) Col. 6: 22, begin running (executing)

See FIG. 1 & 2. Corti disclosed a System on a Chip (SOC), 12. Col. 3: 9-16, The on-chip logic analyzer (OCLA)...is a system for testing and debugging real-time system-on-chip (SOC) systems, e.g., digital signal processing chips..." Col. 3: 27-36, "on-chip VHDL macro 14 (embedded debugger program) embedded in an SOC device 12 (i.e., a target system)...The SOC device 12 includes a signal processing logic (i.e., DSP core / DSP processor) (processor / executing means running a process), memory blocks..." Conti disclosed a process and a debugger program, both of which run on the same processor, the SOC, signal processor / signal processing logic.

Per claim 2:

-the debugger program capturing a trace of the at least part of the executed instructions.

Corti: Col. 3: 56-58, control logic 20 controls the trace buffer 24 to fill up with trace words captured

Per claim 3:

-the computer system includes a port connected to a monitoring system; and further comprising: outputting the captured trace through the port to the monitoring system.

Corti: Col. 3: 36-37, logic captures and transfers the data processed by the signal processing logic to the host system (outputting the captured trace) Col. 4: 6-8, The communication logic 22 provides a communication interface between the data capturing unit 21 and the host system 16. Col. 4: 46, pin 19a for the serial data transfer (port connected to monitoring system)

Per claim 4:

-the process comprises a boot process;

-the instructions comprise boot instructions stored in the ROM of the computer system; and the debugger program is launched from within the boot process.

Corti: Col. 3: 49-52, upon power up (boot instructions) Col. 5: 11-14, power on reset

Per claim 5:

-stopping the execution of the instructions at a first break point;

-the debugger program setting a second break point in the instructions; and continuing the execution of the instructions.

Corti: Col. 5: 21-23, If a '1' is observed on the OCLA_DATA pin 19a, it means the OCLA system 10 has been in the 'RUN' mode and was interrupted (breakpoint). Col. 5: 25, 'continues' See col. 5: 66 – col. 6: 67, various modes may be entered by loading a trigger word to match an mask values (to set break points). Col. 6: 7, "These trigger words 3a, 3b are used to bring important signals out of the DAP core 28 into the data capturing unit 21.

Per claim 7:

-interrupting the execution of the instructions at a current instruction;

-the debugger program operating on the current instruction by disassembling the current instruction; and executing the current instruction.

Corti: Col. 6: 33-42, Trigger on A, store every cycle of the DSP core (disassembling the current instruction), until buffer full condition, empty trace buffer

Per claim 8:

-before executing the current instruction, determining a location of a next instruction of the instructions;

-after executing the current instruction, interrupting the execution of the instructions at the next instruction.

Corti: Col. 5: 67, host system loads the current mode and associated trigger match and mask values (load locations of instructions to interrupt) Col. 6: 56-65, 'A' trigger is met, that cycle of

the DSP core is captured and queued...'B' trigger is met (interrupt at the next instruction), that cycle of the DSP core is captured and queued Col. 8: 11-16

Per claim 9:

-setting a switch within the computer system;

-launching the debugger program in response to detecting the set switch.

Corti: Col. 7: 39-43, hardware debugging FIG. 6 and related text at col. 5: 47, setting bits

Per claim 10:

-setting a break point within the process according to a location specified in a map of the process contained in the debugger program.

Corti: Col. 6: 5-9: loading first and second trigger words FIG. 3 and related text at col. 5: 66

Per claim 11:

A computer system, comprising:

-at least one processor; a read-only memory (ROM) connected to the processor;

-a target process having instructions executable by the processor;

-a debugger program embedded within the ROM, executable by the processor, to operate on at least part of the instructions of the target process.

See rejection of limitations as addressed in claim 1 above.

Per claim 12:

-the target process comprises a boot process.

See rejection of limitations as addressed in claim 4 above.

Per claim 13:

-the debugger program operates on the at least part of the instructions by capturing a trace of the execution of the at least part of the instructions.

See rejection of limitations as addressed in claim 2 above.

Per claim 15:

-the debugger program operates on a current instruction of the target process and sets a break point at a next instruction of the target process to be operated on.

See rejection of limitations as addressed in claim 6 above.

Per claim 16:

-a switch that when set enables launching of the debugger program;

-wherein the target process launches the debugger program upon detecting that the switch is set.

See rejection of limitations as addressed in claim 9 above.

Per claim 17:

-an interrupt flag that when set causes an interruption of execution of the target process;

-wherein, upon interruption of the execution of the target process, the debugger program operates on a current instruction of the target process.

Corti: Col. 6: 32, Trigger on 'A' mode (interrupt flag) Additionally, see rejection of limitations as addressed in claim 7 above.

Per claim 18:

-a map of the target process embedded in the debugger program and specifying locations of parts of the target process.

Corti: Col. 5: 67-Col. 6: 1, load current mode and associated trigger match and mask values

See rejection of limitations as addressed in claim 10 above.

Per claim 19:

A computer debugging system, comprising:

-a target computer; a monitoring system connected to the target computer;

-a data storage device in the monitoring system;

-a read-only memory (ROM) in the target computer;

-a processor in the target computer;

-a target process having instructions executable in the target computer;

-a debugger program embedded in the ROM and executable by the processor in the target computer to generate data on the execution of at least part of the instructions of the target process and to transfer the data to the monitoring system for recording in the data storage device.

Corti: FIG. 2 Col. 2: 59-61, on-chip Col. 3: 43-49, functional units: data capturing unit 21

which includes control logic 20, communication logic 22 and a trace buffer 24...interface logic to the communication logic Col. 3: 56, 'trace buffer, 24' (storage) Col. 3: 26-27, OCLA system 10 includes an on chip VHDL macro 14 embedded in an SOC device Col. 3: 30, memory Col. 2: 29-35, DSP core logic and on chip logic analysis logic (OCLA) Col. 4: 63, DSP instructions performed...

See rejection of limitations as addressed in claims 1, 2, and 3 above.

Per claim 20:

-a disassembler embedded in the ROM and executable in the target computer to disassemble the at least part of the instructions of the target process.

Corti: Col. 7: 63 – Col. 8: 3, The observation is made that specific localized points (nodes) within the VHDL macro 14 is trapped on by monitoring the program counter (PC) value and looking at the various registers and internal busses within the DSP system (disassembling a current instruction) Col. 8: 25-28, To change the location of these software probes (set breakpoints), the developer could simply load the A and B mask values to different program counter values. (calculating where to set second break point). Col. 7: 18, a PC (program counter / address) value Col. 6: 33-42, capture and empty trace buffer by program counter controller

Per claim 21:

-the data on the execution of the at least part of the instructions of the target process comprises a trace capture of the at least part of the instructions.

See rejection of limitations as addressed in claim 3 above.

Per claim 22:

A computer system, comprising: a read-only memory (ROM) means for storing computer control instructions;

-a means for executing a target process;

-a ROM-embedded means for interrupting the execution of the target process at a current instruction, the interrupting means being executable by the target process executing means;

-a ROM-embedded means for disassembling the current instruction, the disassembling means being executable by the target process executing means;

a means for executing the current instruction;

-a ROM-embedded means for capturing a trace of the current instruction and of results of the execution of the current instruction, the trace capturing means being executable by the target process executing means.

Corti: FIG. 2 Col. 4: 52, DSP chip Col. 6: 60-64 Corti disclosed (col. 3: 43-52), "a data capturing unit 21 (trace capturer / trace means)...a trace buffer 24...Upon power-on, the control logic 20 receives control signals designating a mode, a mask value and a match data and a command word..." Col. 3: 53-57, "Once the 'run' bit is the command word is set, the OCLA system 10 starts monitoring the operations of the VHDL macro 14 for trigger conditions...the control logic 20 controls the trace buffer 24... (executable by the processor, DSP core 28) Col. 5: 66 – col. 6: 17 & FIG. 3, "...loads the current mode and associated trigger match and mask values...achieved by loading a trigger word including three 256 bit data words and one command byte...loading of the first trigger word 3a sets an "A" match value, and the second

trigger word 3b holds an "a" mask value. These trigger words 3a, 3b are used to bring important signals out of the DSP core (disassembler) 28 into the data capturing unit 21. Corti fairly teaches a processor (DSP core 28) that executes a disassembler and trace capturer.

Also, see rejection of limitations as addressed in claims 1-7 & 22 above.

Per claim 23:

-a means for transferring the captured trace to an external means for storing the captured trace.

See rejection of limitations as addressed in claim 3 above.

Per claim 24:

A computer system comprising:

-a read-only memory (ROM);

-a target process having executable instructions;

-a debugger program embedded within the ROM and having a disassembler and a trace capturer;

-and wherein: the debugger program interrupts execution of the target process at some of the instructions;

-the disassembler disassembles at least some of the instructions at which the execution of the target process is interrupted;

-and the trace capturer captures a trace of at least some of the disassembled instructions.

See rejection of limitations as addressed in claims 1-7, & 22 above.

Per claim 25:

-the target process comprises a boot process stored within the ROM and having instructions that boot the computer system when the boot process executes.

See rejection of limitations as addressed in claim 4 above.

Per claim 26:

-a port that can be connected to a monitoring system;

-wherein the debugger program outputs the captured trace through the port to the monitoring system.

See rejection of limitations as addressed in claim 3 above.

Per claim 28:

-the computer system executes the current instruction, encounters the break point at the next instruction, and jumps to the debugger program with the next instruction as a new current instruction.

See rejection of limitations as addressed in claims 8 & 9 above.

Per claim 29:

A computer system comprising:

-a switch;

-a processor;

-a target process having executable instructions that are executable by the processor;

-a debugger program that is executable by the processor;

-and wherein: when the switch is off, the debugger program cannot be launched in the processor;

-and when the switch is on, the debugger program can be launched in the processor to interrupt execution of the target process in the processor at some of the instructions and operate on at least some of the instructions at which the execution of the target process is interrupted.

See rejection of limitations as addressed in claim 1 above.

Per claim 30:

A method for debugging a target process executing on a computer system, comprising:

-launching, in a processor of the computer system, a debugger program from a read-only memory (ROM) of the computer system, the ROM having a boot process and the debugger program embedded therein, the debugger program having a disassembler and a trace capturer;

-interrupting execution, in the processor, of the target process at an instruction;

-the disassembler disassembling the instruction; and the trace capturer capturing a trace of the instruction.

See rejection of limitations as addressed in claims 1-7, & 22 above.

Per claim 31:

-executing the instruction; and interrupting the execution of the target process after the instruction.

See rejection of limitations as addressed in claim 8 above.

Per claim 32:

-the target process comprises the boot process.

See rejection of limitations as addressed in claim 4 above.

Per claim 33:

A method for debugging a target process executing on a computer system, comprising:

-setting a switch within the computer system to one of an on state and an off state;

-when the switch is set to the off state, preventing execution of a debugger program in a processor of the computer system;

-when the switch is set to the on state:

-launching the debugger program in the processor;

-interrupting, in the processor, execution of the target process at an instruction;

-the debugger program operating, in the processor, on the instruction.

See rejection of limitations as addressed in claims 1-9 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 14, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,834,360B2 to Corti et al., in view of US Patent 6,694,489 B1 to Case et al.

Per claim 6:

-the debugger program disassembling a current instruction of the instructions;

-determining a length of the current instruction, the length of the current instruction indicating a start point for a next instruction of the instructions;

-setting the second break point at the start point of the next instruction.

Corti: Col. 7: 63 – Col. 8: 3, The observation is made that specific localized points (nodes) within the VHDL macro 14 is trapped on by monitoring the program counter (PC) value and looking at the various registers and internal busses within the DSP system (disassembling a current instruction) Col. 8: 25-28, To change the location of these software probes (set breakpoints), the developer could simply load the A and B mask values to different program counter values. (calculating where to set second break point). Col. 7: 18:, a PC (program counter / address) value

Corti failed to explicitly disclose that one of the trapped values related to the length of the current instruction.

However, Case disclosed a technique for determining the start point for a next instruction of the instructions. (Col. 5: 34-40), The read address pointer as used in the auto-increment command, is updated in the update-dr state with the shifted in read address incremented by the size of the current data. The write address pointer as used in the auto-increment command is updated in the

update-dr state with shifted in write address incremented by the size of the current data. All address bits 31 to 0 are shifted in and updated.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Conti, using the teachings of Case, because (Case: Col. 7: 31-37), a memory auto-increment read/write command reduces the amount of bit-shifts required to perform multiple memory reads or writes by using an internal address pointer from the previous memory read/write command. The auto-increment data size is also set at the same time. The address pointer is incremented by the current data size whenever the internal system bus is granted to the interface internal system bus master.

Per claim 14:

-the debugger program further operates on the at least part of the instructions by disassembling the at least part of the instructions.

See rejection of limitations as addressed in claim 6 above.

Per claim 27:

-the debugger program disassembles a current instruction of the target process, determines a length of the current instruction, and sets a break point at a next instruction of the target process.

See rejection of limitations as addressed in claim 6 above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached at (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned: 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

10/10/2007

MARY STEELMAN
PRIMARY EXAMINER